**Improved Balancing And Sensing of Sub-module Capacitor Voltages In Modular Multi-level Converters Implementation Using Verilog HDL**

**Project Description:** Capacitor voltage balancing is necessary in Modular Multilevel Converters. Voltage controlled oscillator is used for capacitor voltage measurement in reported literature where voltage sensor is required to be calibrated. In the present work, a voltage sensing method that does not need calibration of individual voltage sensors is used for capacitor voltage measurement. Open loop phase shifted carrier pulse width modulation (PSCPWM) method is used and sorting algorithm is employed for capacitor voltage balance. A method of sorting capacitor voltages that selects the modules to be inserted directly based on logic equations is used as compared to the conventional methods of arranging them in ascending or descending order. This facilitates use of Field Programmable Gate Array for sorting. Fairly good capacitor voltage balance is obtained.

**Aim:** To design a MMC of 7 level(6 capacitors in each branch) by implementing a Verilog module that takes the input voltage of all capacitor and the number of capacitor to be turned ON in upper branch. It should output an array of length 12 where each bit represents status of each capacitor (if it is tuned ON or bypassed).

I have used IEEE 754 single precision floating point number to represent current and voltages.

**References:** <https://ieeexplore.ieee.org/document/8558331>

**Observations:**

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| **SL No** | **Testcase Description** | **Output** |
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**In all cases our outcomes meet the expected result.**